DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the fragmentary sectional view of the semiconductor integrated circuit for explaining the principle of operation of the static protection circuit concerning this invention.
[Drawing 2] It is a circuit diagram for explaining the principle of operation of the static protection circuit shown in drawing 1 . That is, drawing 2 (a) is the representative circuit schematic of the static protection circuit shown in drawing 1 , and drawing 2 (b) is the representative circuit schematic of the parasitism bipolar transistor 30 of the static protection circuit shown in drawing 1 .
[Drawing 3] It is the simple property view having shown the state of the voltage at the time of operation of the static protection circuit concerning this invention. That is, drawing 3 (a) is the simple property view having shown the state of the voltage at the time of operation of the static protection circuit concerning this invention when positive surge voltage is impressed to a high-voltage side edge child, and drawing 3 (b) is the simple property view having shown the state of the voltage at the time of operation of the static protection circuit concerning this invention when negative surge voltage is impressed to a low-battery side edge child.
[Drawing 4] It is partial drawing of longitudinal section of a semiconductor integrated circuit showing concretely one gestalt of operation of the static protection circuit concerning this invention.
[Drawing 5] It is partial drawing of longitudinal section of a semiconductor integrated circuit showing concretely other gestalten of operation of the static protection circuit concerning this invention.
[Drawing 6] It is partial drawing of longitudinal section of a semiconductor integrated circuit showing concretely one gestalt of operation of a semiconductor integrated circuit including the static protection circuit concerning this invention.
[Drawing 7] It is the representative circuit schematic of the semiconductor integrated circuit shown in drawing 6 .
[Drawing 8] it is the fragmentary sectional view of the semiconductor integrated circuit for explaining the principle of operation of a punch-through use type circuit among the electrostatic protection networks by the Prior art which used N channel MOSFET
[Drawing 9] It is the representative circuit schematic of the semiconductor integrated circuit shown in drawing 8 .
[Drawing 10] It is the simple property view having shown the state of the voltage at the time of operation of the semiconductor integrated circuit shown in drawing 8 . That is, drawing 10 (a) is the simple property view having shown the state of voltage when positive surge voltage is impressed to the high-voltage side edge child 95, and drawing 10 (b) is the simple property view having shown the state of voltage when negative surge voltage is impressed to the low-battery side edge child 96.
[Drawing 11] it is the fragmentary sectional view of the semiconductor integrated circuit for explaining the principle of operation of an N channel MOSFET operation use type circuit among the electrostatic protection networks by the Prior art
[Drawing 12] It is the representative circuit schematic of the semiconductor integrated circuit shown in drawing 11 .
[Description of Notations]
10 97 Capacitor
20 98 Quantity resistance
30 Parasitism Bipolar Transistor
50 Base Current of Parasitism Bipolar Transistor
55 ON Current of Parasitism Bipolar Transistor
67 N Channel
80 N-type Semiconductor Substrate
81 81' P well
82 Drain
83 Source
84 Gate
85 P+ Impurity Diffusion Field
86 N+ Impurity Diffusion Field
87 Insulating Layer
88 P Channel MOS
89 90,100 N channel MOS
91 Punch-through Current
94 Connection between P+ Impurity Diffusion Field 85 and 85

95 High-Voltage Side Edge Child
96 Low-Battery Side Edge Child
99 ON Current of NMOS90

[Translation done.]